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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/805,609 | 03/19/2004 | David Bistry | 42P2737C4 | 9498 |

8791 7590 06/27/2007

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| EXAMINER | |
|---|---|
| COLEMAN, ERIC | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 06/27/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/805,609 | BISTRY ET AL. | |
| | Examiner | Art Unit | |
| | Eric Coleman | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-23 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Double Patenting*

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-7,8-15 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 31,37 of U.S. Patent No. 6,751,725.

Claims 16-23 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 11,13, of U.S. Patent No. 6,266,686.

Although the conflicting claims are not identical, they are not patentably distinct from each other because as the patent claims contain features of the claims in the instant case as shown by the side by side display shown below.

| Patent 6,751,725 | Instant application |
| --- | --- |
| 31. A computer-implemented method comprising: executing a first block of code including scalar floating point instructions and no packed data instructions, at least certain of said scalar floating point instructions specifying operating with reference to a top of a stack, wherein each of a plurality of tags is associated with a different entry in said stack, said plurality of tags indicating either empty or non-empty responsive to execution of scalar floating point instructions that cause data contained in said stack to be modified; and executing a second block of code including packed data instructions, no scalar floating point instructions, and concluding with a single instruction, said packed data instructions specify registers in a non-stack referenced manner, wherein execution of said single instruction causes all of said plurality of tags to be altered to indicate empty. | 1. A machine readable medium stored thereon a plurality of control signals and when accessed by a processor causing said processor to: access a first set of bits as representing an instruction of a first plurality of instructions, said plurality of instructions including a packed data instruction, a scalar floating point instruction and a transition instruction to be executed between the packed data instruction and said scalar floating point instruction; if said first set of bits represents the packed data instruction then generate a first set of control signals to cause said processor to execute the packed data instruction on packed data contents of a storage representing a programmer visible register file, wherein said storage representing the programmer visible register file is operated as a flat register file while executing said packed data instruction; if said first set of bits represents the scalar floating point instruction then generate the first set of control signals to cause said processor to execute the scalar floating point |

Patent 6,751,725

37. The computer-implemented method of claim 31, wherein execution of said single instruction also causes initializing of a top of stack indication for said stack.

Instant application

instruction on floating point contents of the storage representing programmer visible file, wherein said programmer visible register file is operated as a stack while executing said scalar floating point instruction; and if said first set of bits represents the transition instruction then generate the first set of control signals to cause said processor to alter a tag data to indicate that the stack of the programmer visible register file is empty responsive to executing said transition instruction between execution of said packed data instructions and said scalar floating point instruction.

3. the machine readable medium o f claim 1, when accessed by said processor, further causing the processor to alter a top of stack to indicate that top of the stack of the programmer visible register file is zero if said first set of bits represents the transition instruction or if said first set of bits represents said packed data instruction.

| Patent 6,751,725 | Instant application |
| --- | --- |
| 31. A computer-implemented method comprising: executing a first block of code including scalar floating point instructions and no packed data instructions, at least certain of said scalar floating point instructions specifying operating with reference to a top of a stack, wherein each of a plurality of tags is associated with a different entry in said stack, said plurality of tags indicating either empty or non-empty responsive to execution of scalar floating point instructions that cause data contained in said stack to be modified; and executing a second block of code including packed data instructions, no scalar floating point instructions, and concluding with a single instruction, said packed data instructions specify registers in a non-stack referenced manner, wherein execution of said single instruction causes all of said plurality of tags to be altered to indicate empty. | 8. A computer-implemented method comprising:<br>accessing a first set of bits as representing a packed data instruction; storing a first corresponding set of control bits to cause a processor to alter a top of stack data to zero and to operate on packed data contents of a storage representing a programmer visible register file as a flat register file; accessing a second set of bits as representing a scalar floating point instruction; storing a second corresponding set of control bits as representing a scalar floating point instruction; storing a second corresponding set of control bits to cause the processor to operate on floating point data contents of the storage representing the programmer visible register file as a stack; accessing a third set of bits as representing a transition instruction to be executed between said packed data instruction and said scalar floating point instruction; and storing a third corresponding set of control bits to cause the processor to alter a tag data to indicate that the stack of the programmer visible register file is empty.<br>13. the computer implemented method of claim 9, wherein the third set of control bits further causes said processor toe alter the top of stack data to indicate that top of the stack programmer visible file is zero. |

| Patent No. 6,266,686 | Instant application |
| --- | --- |
| 11. A computer system comprising:<br><br>a processor including a set of registers to store environment information related to a shared architecturally visible register file, said environment information including data for accessing said shared architecturally visible register file in a stack referenced manner and data related to exceptions;<br><br>a bus coupled to said processor;<br><br>a memory coupled to said bus; and<br><br>a disk drive coupled to said bus having stored thereon a plurality of instructions, said plurality of instructions including packed floating point instructions, followed by a single transition instruction, followed by scalar floating point instructions, said plurality of instructions, when executed by said processor, causing said processor to,<br><br>execute said packed floating point instructions and said scalar floating | 16. A computer system comprising:<br>a processor execution unit to execute control signals: bus coupled with said processor execution unit configurable to access one or more machine readable medium; first machine readable medium configurable to store a first plurality of instructions, said first plurality of instructions including a packed data instruction, a scalar floating point instruction, and a transition instruction to be executed between said packed data instruction, and a transition to be executed between said packed instruction and said scalar floating point instruction; second machine readable medium configurable to store a programmable visible register file and related environment information, said environment information including a tag data and a top of stack data for accessing said programmable visible register file in a stack referenced manner; and a third machine readable medium having stored thereon a plurality of control signals that, when accessed by the processor execution unit, cause said processor execution unit to, access a first set of bits as |

Patent No. 6,266,686

point instructions on the contents of said shared architecturally visible register file, wherein said shared architecturally visible register file is operated as a flat register file while executing said packed floating point instructions, wherein said shared architecturally visible register file is operated as a stack while executing said scalar floating point instructions;

alter said data for accessing said architecturally visible register file to indicate the stack is empty responsive to executing said single transition instruction between execution of said packed floating point instructions and said scalar floating point instructions.

13. The computer.system of claim 11, wherein execution of said single transition instruction also causes clearing of a top of stack indication for said stack.

Instant application

Representing an instruction of the first plurality of instructions from the first machine readable medium, generate a first set of control signals to cause said processor execution unit to alter the top of stack data to zero and operate on contents of the programmer visible register file as a flat register file when said first set of bits represents the packed data instruction, generate the first set of control signals to cause said processor execution unit to operate on contents of the programmer visible register file in a stack referenced manner when said first set of bits represents the scalar floating point instruction and generate the first set of control signals to cause said processor execution unit to alter tag data to indicate that the stack of the programmer visible register file is empty when said first set of bits represents the transition instruction.

As can be seen by the side by side display of the corresponding claims above, they are direct to the same inventive concept. The Examiner contends that the portions of the claims of the instant application that were not explicitly detailed in the corresponding patent claims are aspect that would have been obvious and within the level of skill of one of ordinary skill at the time of the claimed invention to implement in the claimed invention of respective patented claims. As to claims 1,8,16 of the instant application, access to bits that represent the instruction in the patented claims would have been required when processing instructions in the patented claimed invention.

Further each patented claimed invention included (single) the transition instruction followed the packed data instruction and therefore when execution the instructions between the packed data instruction and scalar floating point instruction would have had to have been the single (transition) instruction. Further as to the generation of controlling signals the processing of instruction would required generating the corresponding control signals to control the system to perform the operations of the instructions. Also the register file of the claimed invention would have stored instructions for programming the system (without any indication that the access to the program would have been restricted) and therefore would have been a programmer visible register file.

Further as to claims 16,19,22-23 of the instant application, the first, second, and third machine readable medium configurable to store ... or storing control signals, both patented claimed processors would have required storing the instructions and the patent claims included a register file and in order to implement the instructions the

processor would have had to have circuitry that would have contained the controlling signals so that the signals could be sent to a required portion of the execution unit in a properly timed manner. In the processing of instruction, decoded instructions would have produced microcode signals. Here one of ordinary skill would have been motivated to use conventional off the shelf mediums such as ROM and DRAM at least because these would have been readily available.

As to the limitations of claims 2,9, since when a packed data operation of the patented claims was to be performed the system would have operated on data in a different manner and in a different grouping or size of data then one of ordinary skill would have been motivated to change the data within the register to indicate to the system that the data was format or grouping was different from the format of the number when scalar floating point processing was being performed. As to the limitations of claims 4-6,10-12,18,20,21 of this application, these are merely intended use for the data and since the patented claims provided different types of processing then one of ordinary skill would have been motivated to output this data to various corresponding types of conventional processing systems namely RISC, CISC and VLIW.

As per claims 7,14,15,17 of this application, The one of ordinary skill would have been motivated to save one context when switching to another context in the invention claimed in the patents as the system processes instructions of different types that required different type of memory organization. Otherwise the system would lose the contextual (i.e., results and status) information when the switching from one type such as packed instruction to scalar floating point instruction. Without the ability to save the

packed data instruction status and results the register file could not be changed from a flat organization to a stacked organization without losing all the status and results obtained by processing in the flat organization. One of ordinary skill also would have been motivated to use a save instruction to implement the save at least because it provides flexibility to the programmer as to when to save. Using save instruction the instruction would have to have been decoded to produce control signals to implement the save. Also the system would have required a indication (either implicit or explicit) for when the save was completed so that the instruction using to other register organization could begin and one of ordinary skill would have been motivated to zero or initialize the memory when changing configuration at least to ensure that that no garbage data remained in the register file when used by the instruction with the other register configuration.

Also claim 33, of patent 6,751,725 comprises "wherein execution of any of said packed data instructions cause said plurality of tags to be altered to indicate non-empty". In patent No. 6,266,686 claim 11 comprises "alter said data for accessing architecturally visible register file to indicate the stack is empty". This shows that the claimed invention comprises tags and that the tags indicated whether the register file locations are empty or not.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kogge (patent No. 5,475,856) disclosed dynamic multimode processing array (e.g., see abstract).

Kelly (patent No. 5,996,036 ) disclosed a bus transaction reordering in a computer system having unordered slaves (e.g., see abstract).

Jen (patent No. 5,031,096) disclosed a system for compressing the execution time of instruction stream executing in a pipelined processor (e.g., see abstract).

Buerkle (patent No. 5,099,421) disclosed variable sequencing pipeline with a stack mode and non-stack mode (e.g., see abstract).

Colley (patent No. 5,113,523) disclosed a high performance computer system various addressing modes (e.g., see abstract and col. 34, line 8-col. 38, line 38).

Taylor (patent No. 5,664,214) disclosed a parallel processing computer containing a multiple instruction stream processing architecture (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC

ERIC COLEMAN
PRIMARY EXAMINER